AMENDMENTS TO THE CLAIMS

Kindly amend the claims as follows:

1. (currently amended) In a telecommunication system split into a plurality of subsystems ~~adapted~~ to exchange serial data bits arranged in frames n bits long (n-bit frames) according to ~~the~~ a dynamic time division multiplexing (TDM) access method wherein the time is split in time slots, so that to each bit position (Bit1 to Bitn) of said frame is associated either one among N logical channels or a null value, N being the maximum number of logical channels ~~(...,X,...)~~ that can be simultaneously opened and wherein to each logical channel (X) is associated an identifier (LC X) coded on p bits where N, n and p are integers, wherein the improvement ~~comprising~~comprises:

first data storage means comprising an n x p memory block to store ~~the~~ a time slot assignment (TSA) table which specifies for each bit position of the n-bit frame, the logical channel it belongs to at a given time, describing thereby the different time slots ~~(TimeslotX,.....)~~;

second data storage means comprising a N x 1 register to store status bits that indicates for each logical channel its status, "assigned" when it has a first value or "unassigned" when it has another value;

input bus means for inputting the logical channel identifiers into said first data storage means and the value of the status bits in said second data storage means from a computer or an application software; and,

logic circuit means connected to said first and second data storage means that enables or disables the transmission of the logical channel identifiers

depending upon they are “assigned” or “unassigned” to an output bus means for subsequent processing by a time slot assignor.

2. (currently amended) The telecommunication system according to claim 1 wherein the null value corresponds to a bit position to which ~~none~~ no logical channel is assigned.

3. (new) The system of claim 1 wherein said logic circuit means comprises p parallel two-way AND gates.

4. (new) The system of claim 3 wherein said AND gates receive inputs from said memory block and from said register.

5. (new) The system of claim 4 wherein each AND gate receives one of p bits from a channel identifier data entry in said TSA table.

6. (new) A method for providing logical channel identifier information to a time slot assignor in a dynamic time division multiplexing process, said method comprising:

splitting time into time slots, each slot corresponding to one among N logical channels, wherein N is a maximum number of logical channels that can be simultaneously opened in said process,

storing in an N x p memory block time slot assignment (TSA) table at least one identifier (LC X) associated with logical channel (X), each said identifier being coded on p bits, specifying each bit position of an n-bit TDM frame that is assigned to said logical channel,

storing status bits a register having N fields with a granularity of one bit, each bit indicating the status of a corresponding identifier in said TSA table, and

transmitting said at least one identifier from said TSA table to a time slot assigner, wherein said transmission is controlled by a logic circuit receiving data from said resister as an input thereto.

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